Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

Claims 1-42 (canceled)

43. (currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprise a first metal layer and a second metal layer over said first metal layer;

a first dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said first dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure and exposes said first contact point, and a second opening in said passivation layer is over a second contact point of said metallization structure and exposes said second contact point, wherein said first and second contact points are separated from each other by an insulating material, and wherein said passivation layer comprises silicon nitride; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, and wherein said circuit trace is connected to said resistor through said first opening.

44. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises boron.

45. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises phosphorous.

46. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises arsenic.

47. (previously presented) The chip structure as claimed in claim 43, wherein said dopant comprises gallium.

48. (currently amended) The chip structure as claimed in claim 43 further comprising a polymer layer between said ~~silicon nitride~~ passivation layer and said circuit trace.

49. (previously presented) The chip structure as claimed in claim 48, wherein said polymer layer comprises polyimide (PI).

50. (previously presented) The chip structure as claimed in claim 48, wherein said polymer layer comprises benzocyclobutene (BCB).

51. (previously presented) The chip structure as claimed in claim 43 further comprising a polymer layer on said circuit trace.

52. (previously presented) The chip structure as claimed in claim 51, wherein said polymer layer comprises polyimide (PI).

53. (previously presented) The chip structure as claimed in claim 51, wherein said polymer layer comprises benzocyclobutene (BCB).

54. (currently amended) The chip structure as claimed in claim 43 further comprising an inductor over said passivation layer. ~~, wherein said circuit trace comprises a copper layer.~~

55. (currently amended) The chip structure as claimed in claim 54, wherein said inductor ~~circuit trace further~~ comprises a ~~nickel layer over said~~ copper layer.

56. (currently amended) The chip structure as claimed in claim 54, wherein said inductor ~~circuit trace further~~ comprises a gold layer ~~over said copper layer~~.

57. (currently amended) The chip structure as claimed in claim 54, wherein said inductor ~~circuit trace further~~ comprises a copper layer and a titanium-containing layer under said copper layer.

58. (previously presented) The chip structure as claimed in claim 57, wherein said titanium-containing layer comprises tungsten.

59. (currently amended) The chip structure as claimed in claim 43 ~~54,~~ further comprising a capacitor over said silicon substrate, wherein said capacitor comprises a first electrode over said silicon substrate, a second electrode over said first electrode, and a second dielectric layer between said first and second electrodes, wherein a third opening in said passivation layer is over said first electrode and exposes said first electrode. ~~wherein said circuit trace further comprises a chromium-containing layer under said copper layer.~~

60. (currently amended) The chip structure as claimed in claim 59, ~~43,~~ wherein said second electrode ~~circuit trace~~ comprises a gold layer.

61. (currently amended) The chip structure as claimed in claim 60, wherein said second electrode ~~circuit trace~~ further comprises a titanium-containing layer under said gold layer.

62. (currently amended) The chip structure as claimed in claim 59, ~~61,~~ wherein said second electrode ~~titanium-containing layer~~ comprises a copper layer. ~~tungsten.~~

63. (currently amended) The chip structure as claimed in claim 59, ~~43,~~ wherein said second electrode ~~metallization structure~~ comprises a copper layer and a nickel layer over said copper layer. ~~aluminum.~~

64. (currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure and exposes said first contact point, and a second opening in said passivation layer is over a second contact point of said metallization structure and exposes said second contact point, wherein said first and second contact points are separated from each other by an insulating material, and wherein said passivation layer comprises silicon nitride; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor,

through said first opening, and wherein said circuit trace comprises a titanium-containing layer and a gold layer over said titanium-containing layer.

65. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises boron.

66. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises phosphorous.

67. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises arsenic.

68. (previously presented) The chip structure as claimed in claim 64, wherein said dopant comprises gallium.

69. (previously presented) The chip structure as claimed in claim 64 further comprising a polymer layer between said passivation layer and said circuit trace.

70. (previously presented) The chip structure as claimed in claim 69, wherein said polymer layer comprises polyimide (PI).

71. (previously presented) The chip structure as claimed in claim 69, wherein said polymer layer comprises benzocyclobutene (BCB).

72. (previously presented) The chip structure as claimed in claim 64 further comprising a polymer layer on said circuit trace.

73. (previously presented) The chip structure as claimed in claim 72, wherein said polymer layer comprises polyimide (PI).

74. (previously presented) The chip structure as claimed in claim 72, wherein said polymer layer comprises benzocyclobutene (BCB).

Claims 75-82 (canceled)

83. (previously presented) The chip structure as claimed in claim 64, wherein said titanium-containing layer comprises tungsten.

84. (previously presented) The chip structure as claimed in claim 64, wherein said metallization structure comprises aluminum.

Claims 85-88 (canceled)

89. (currently amended) A chip structure comprising:

a silicon substrate;

a resistor in said silicon substrate, wherein said resistor comprises silicon with a dopant;

a MOS device comprising a portion in said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a passivation layer over said metallization structure and over said dielectric layer, wherein a first opening in said passivation layer is over a first contact point of said metallization structure and exposes said first contact point, and a second opening in said passivation layer is over a second contact point of said metallization structure and exposes said second contact point, wherein said first and second contact points are separated from each other by an insulating material, and wherein said passivation layer comprises silicon nitride; and

a circuit trace over said passivation layer and over said first and second contact points, wherein said first contact point is connected to said second contact point through said circuit trace, wherein said circuit trace is connected to said resistor through said first opening, and wherein said circuit trace comprises ~~a third metal layer and~~ a copper layer ~~over said third metal layer~~.

90. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises boron.

91. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises phosphorous.

92. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises arsenic.

93. (previously presented) The chip structure as claimed in claim 89, wherein said dopant comprises gallium.

94. (previously presented) The chip structure as claimed in claim 89 further comprising a polymer layer between said passivation layer and said circuit trace.

95. (previously presented) The chip structure as claimed in claim 94, wherein said polymer layer comprises polyimide (PI).

96. (previously presented) The chip structure as claimed in claim 94, wherein said polymer layer comprises benzocyclobutene (BCB).

97. (previously presented) The chip structure as claimed in claim 89 further comprising a polymer layer on said circuit trace.

98. (previously presented) The chip structure as claimed in claim 97, wherein said polymer layer comprises polyimide (PI).

99. (previously presented) The chip structure as claimed in claim 97, wherein said polymer layer comprises benzocyclobutene (BCB).

100. (currently amended) The chip structure as claimed in claim 89, wherein said circuit trace further ~~third metal layer~~ comprises a nickel layer over said copper layer. ~~titanium.~~

101. (currently amended) The chip structure as claimed in claim 89, wherein said circuit trace further ~~third metal layer~~ comprises a gold layer over said copper layer. ~~chromium.~~

102. (currently amended) The chip structure as claimed in claim 89, wherein said circuit trace further ~~metallization structure~~ comprises a nickel layer over said copper layer, and a gold layer over said nickel layer. ~~aluminum.~~